

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

1. (Previously Presented) A method for processing integrated circuit devices, the method comprising:

providing a monitor wafer, the monitor wafer comprising a silicon material;  
introducing a plurality of particles within a depth of the silicon material,  
whereupon the plurality of particles cause the silicon material to be in an amorphous state;  
introducing a plurality of dopant particles into a selected depth of the silicon material using an implantation tool, the amorphous state trapping the dopant particles;  
subjecting the monitor wafer including the plurality of particles and dopant particles into thermal anneal process to activate the dopant;  
removing the monitor wafer;  
measuring a sheet resistivity of a surface region including the implanted dopant particles of the monitor wafer;  
determining a dose of the dopant bearing impurities; and  
operating the implantation tool using one or more production wafers if the dose of the dopant particles in the monitor wafer is within a tolerance of a specification limit.

2. (Original) The method of claim 1 wherein the monitor wafer is substantially free of screen oxide overlying a surface of the monitor wafer.

3. (Previously Presented) The method of claim 1 wherein the plurality of particles are silicon bearing species.

4. (Previously Presented) The method of claim 3 wherein the silicon bearing species are implanted using a dose of  $1 \times 10^{15}$  atoms/cm<sup>2</sup> and an energy of 20 keV.

5. (Original) The method of claim 1 wherein the dopant particles are boron bearing impurities.

6. (Previously Presented) The method of claim 5 wherein the boron bearing impurities are implanted using a dose ranging from about  $4 \times 10^{14}$  through  $1 \times 10^{15}$  atoms/cm<sup>2</sup> and an energy ranging from about 1-2 keV.

7. (Original) The method of claim 1 wherein the thermal anneal process is an RTP process at about 700 Degrees Celsius.

8. (Original) The method of claim 1 wherein the thermal anneal process is an RTP process ranging from about 650 to 750 Degrees Celsius.

9. (Original) The method of claim 1 wherein the thermal anneal process is a rapid thermal anneal process.

10. (Original) The method of claim 1 wherein the sheet resistivity is provided in a separate tool.

11. (Currently Amended) The method of claim 1 wherein the operating of the ~~production wafers implantation tool~~ occurs for 24 hours after determining the dose of the dopant impurities.

12. (Original) The method of claim 1 wherein the thermal anneal process also recrystallizes a portion of the amorphous silicon.

13. (Previously Presented) A method for processing semiconductor wafers, the method comprising:

providing a monitor wafer, the monitor wafer comprising a crystalline material;  
introducing a plurality of particles within a depth of the material, whereupon the plurality of particles cause the crystalline material to be in an amorphous state;

introducing a plurality of dopant particles into a selected depth of the crystalline material in the amorphous state using an implantation tool, the amorphous state trapping the dopant particles;

subjecting the monitor wafer including the plurality of particles and dopant particles into thermal anneal process to activate the dopant;

removing the monitor wafer;

measuring a sheet resistivity of a surface region including the implanted dopant particles of the monitor wafer;

determining a dose of the dopant bearing impurities; and

operating the implantation tool using one or more production wafers if the dose of the dopant particles in the monitor water is within a tolerance of a specification limit.

14. (Previously Presented) The method of claim 13 wherein the crystalline material comprises silicon.

15. (Previously Presented) The method of claim 13 wherein the dose of the dopant bearing impurities is determined using a relationship between resistivity values and dose values.

16. (Previously Presented) The method of claim 15 wherein the relationship has been provided in a spatial plot.

17. (Previously Presented) The method of claim 13 wherein the plurality of particles comprise silicon bearing particles.

18. (Previously Presented) The method of claim 13 wherein the dopant bearing impurities comprise boron species.

19. (Previously Presented) The method of claim 13 wherein the monitor water is substantially free from an overlying oxide layer before introducing the dopant bearing impurities.

20. (Previously Presented) The method of claim 13 wherein the monitor wafer is a silicon wafer.

21. (Previously Presented) The method of claim 13 wherein the one or more production wafers is characterized by a shallow junction depth of less than about 40 nm.